UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,688	10/11/2005	Tatsuya Fujii	2271/75306	3791

23432 7590 04/27/2010

COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

EXAMINER	
RUTKOWSKI, JEFFREY M	
ART UNIT	PAPER NUMBER
2473	

MAIL DATE	DELIVERY MODE
04/27/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,688	FUJII, TATSUYA	
	Examiner	Art Unit	
	JEFFREY M. RUTKOWSKI	2473	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8,11,12 and 30-33* is/are rejected.

7)☒ Claim(s) *2-7,9,10 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 13-29 have been cancelled.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1, 11-12 and 30-33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattern (US Pat 4,063,200), in view of Tanabe (US Pg Pub 2003/0174737).

4. For **claim 1**, Mattern discloses *a sending part* (multipliers **17, 18 and 19** and summing device **28**; see figure 1) *for converting an amplitude of each of the plurality of digital input signals* (items **20, 21 and 22**; see figure 1) *into a weighted voltage* (a product voltage; see col. 3 lines 1-5, col. 5 lines 4-10) *in accordance with a predetermined weight* (binary numbers on inputs **14, 15 and 16**; see col. 2 lines 54-57. Outputs **25, 26 and 27** of the multipliers **17, 18 and 19** output a converted voltage of the input signals **20, 21 and 22** that is weighted by the binary numbers **14, 15 and 16**; see col. 3 lines 1-5), *and generating a send signal by adding the*

weighted voltages converted from the plurality of digital input signals (the voltages from outputs **25, 26 and 27** are fed into a summing device **28**; see col. 3 lines 5-6 and col. 5 lines 4-10)*, and outputting the send signal* (the information is sent from the summing device **28** to a demultiplexer; see col. 2 lines 20-26).

5. Mattern discloses *a receiving part* (demultiplexer **38**; see figure 1) *for receiving the send signal from the sending part* (see col. 2 lines 20-26)*, generating a plurality of digital output signals* (discrete output) *corresponding to the plurality of digital input signals* (each discrete output corresponds to a representative input frequency; see col. 2 lines 14-27)*, based on the send signal* (the output of the demultiplexer **38** is based on the input from the weighted samples that were sent from the summing device **28**; see col. 2 lines 14-27, *and outputting said plurality of the digital output signals* (the demultiplexer **38** produces discrete outputs; see col. 2 lines 20-27). Mattern does not disclose a demultiplexer **38** that has a comparator. Tanabe discloses a demultiplexer (see figure 6) that *compares a send signal* (the output of adding circuit **11**; see figure 8); *with a plurality of predetermined reference voltages* (comparing circuits **12-1 and 12-2** compare the output of the adding circuit **11** with reference voltages H and L; see paragraph 0078). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Tanabe's demultiplexer circuit in Mattern's invention to accurately read serial data at a higher data rate (Tanabe, paragraph 0010).

6. For **claim 11**, Mattern does not disclose a demultiplexer **38** that has a comparator. Tanabe discloses *a reference voltage generating circuit for generating and outputting each of the plurality of predetermined reference voltages* (figure 8 shows the use of separate reference generating circuits)*; a voltage comparing circuit for comparing each of the plurality of*

predetermined reference voltages and the send signal received from said sending part (the comparing circuit **12** compares the reference voltages to the signal received from the adding circuit **12**; see figure 8), *and outputting a plurality of comparison signals showing each comparison result* (each result of the comparison circuit is output on lines CH and CL; see figure 8); *and a logic circuit for synthesizing each of the digital signals based on the plurality of comparison signals of said voltage comparing circuit in accordance with a predetermined method* (the D-latches **13** synthesize the results from the comparison circuit; see figure 8). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Tanabe's demultiplexer circuit in Mattern's invention to accurately read serial data at a higher data rate (Tanabe, paragraph 0010).

7. For **claim 12**, Mattern does not disclose a demultiplexer **38** that has a comparator. Tanabe suggests *wherein in a case of two digital input signals* (plurality of inputs bits; see paragraph 0033. The adding circuit **11** adds two input bits at a time; see figure 9), *the plurality of comparison the voltage comparing circuit are equal to the plurality of digital input signals* (for every two bits added two comparison signals are output; see figures 8 and 9), *and said logic circuit directly outputs the plurality of comparison signals received from the voltage comparing circuit* (the latches **13** directly output the comparison signals that are received from the comparing circuit **12**; see paragraph 0078 and figure 8).

8. For **claim 30**, Mattern discloses *wherein the send signal is transmitted from the sending part* (multipliers **17, 18 and 19** and summing device **28**; see figure 1) *to the receiving part* (demultiplexer **38**), *through the single signal line* (item **37**; see figure 1).

9. For **claim 31**, Mattern discloses *wherein a value of the send signal generated by adding the weighted voltages converted from the plurality of digital input signals uniquely corresponds to values of the digital inputs signals* (each discrete output corresponds to a representative input frequency; see col. 2 lines 14-27), *such that said values of the digital input signals can be determined based solely on said value of the send signal* (see col. 2 lines 21-27).

10. For **claim 32**, Mattern does not disclose a demultiplexer **38** that has a comparator. Tanabe discloses a demultiplexer (see figure 6) that *compares a send signal* (the output of adding circuit **11**; see figure 8) *with a plurality of predetermined reference voltages* (comparing circuits **12-1 and 12-2** compare the output of the adding circuit **11** with reference voltages H and L; see paragraph 0078). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Tanabe's demultiplexer circuit in Mattern's invention to accurately read serial data at a higher data rate (Tanabe, paragraph 0010).

11. For **claim 33**, Mattern discloses *wherein a first weighting or first multiplication factor* (G) *is used to convert a first amplitude of a first one of the digital input signals* (signal on input line **20**) *into a first weighted voltage* (the multiplier **17** uses G as a constant; see figure 1), *and wherein a second weighting or second multiplication factor* (K1), *different from the first weighting or fast multiplication factor* (G and K1 are different; see col. 5 line 65 to col. 6 line 7), *is used to, convert a second amplitude of a second one of the digital input signals* (input on line **21**) *into a second weighted voltage* (the multiplier **18** uses K1 as a constant; see figure 1).

12. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Mattern in view of Tanabe as applied to **claim 1** above, and further in view of Yoshino (US Pat 5,499,269).

13. For **claim 8**, the combination of Mattern and Tanabe discloses *wherein said sending part* (multipliers **17, 18 and 19** and summing device **28**; see figure 1) *adds the voltages being converted* (the voltages from outputs **25, 26 and 27** are fed into a summing device **28**; see col. 3 lines 5-6 and col. 5 lines 4-10).

14. The combination of Mattern and Tanabe does not disclose using a signal with a greatest weight as a predetermined signal level. Yoshino suggests *a digital input signal having a greatest weight in the digital input signals is a predetermined signal level* (a comparison is performed between signals that have been added and a threshold value to extract only one signal that was sent; see col. 2 lines 5-10). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a signal with a greatest weight as a predetermined signal level in Mattern's invention to distinguish one signal from another (Yoshino, col. 2 lines 5-10).

Response to Arguments

15. Applicant's arguments with respect to **claims 1, 8, 11-12 and 30-33** have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

16. **Claims 2-7, 9-10 and 34** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The following is a statement of reasons for the indication of allowable subject matter:

a. For **claims 2-5 and 34**, the cited prior art does not teach or suggest the circuit arrangement that is required by **claim 2**. Additionally, the circuit arrangement in Mattern's figure 1 and Tanabe's figure 6 teaches away from the circuit arrangement in

claim 2 because neither Mattern's nor Tanabe's invention uses resistors in the sending and receiving parts.

b. For **claims 6-7**, the combination of Mattern and Tanabe discloses the use of more than one reference voltage (see figure 8). The cited prior art does not teach or suggest the use of an algorithm to determine the number of reference voltages to use as required by **claim 6**.

c. For **claims 9-10**, the reasons for allowance for these claims is the same as the reasons for allowance for **claims 2-5 and 34** above.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY M. RUTKOWSKI whose telephone number is (571)270-1215. The examiner can normally be reached on Monday - Friday 7:30-5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeffrey M Rutkowski/
Examiner, Art Unit 2473

/KWANG B. YAO/

Supervisory Patent Examiner, Art Unit 2473